AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Please replace the Abstract with the following amended Abstract:

An electronic Input/Output Interface and device abstraction system used in gaming machine includes: a game central processing unit (the game "CPU"); an intelligent input/output controller board (the "IOCB"); an Industry Standard Architecture PC bus (~~"IBA"~~ "ISA" bus); and a framed message transport protocol. The IOCB facilitates the communications between the game CPU and virtual device services, which[[,]] are peripheral devices associated with the gaming system. These include devices such as displays, buttons, hoppers, coin mechanisms and bill validators. The framed message transport protocol includes: a message header, a body containing a virtual device message, and a packet validation signature. The game CPU communicates to gaming peripherals by sending virtual device messages across the ISA bus to the IOCB. The IOCB then routes the virtual device message to the appropriate virtual device services. The virtual device services are responsible for handling specific hardware, and are made up of virtual device drivers on the game CPU that communicate with virtual devices on the IOCB and use of the IOCB and the high speed interface enables the game CPU to use more of its available functions for controlling gaming functions rather than one operation of its associated peripheral devices.

Please replace the paragraph in the Background of the Invention on page 2, lines 7-12 with the following amended paragraph:

The present invention describes communications between the game CPU and the ~~IOCG~~ IOCB. A factor in establishing reliable communications between the game CPU and the ~~IOCG~~ IOCB is having properly abstracted hardware to allow the software on the game

CPU to adapt and correspond to new hardware arrangements with fewer changes to the game CPU hardware and software. The present invention further describes the hardware abstraction protocol.

Please replace the paragraph in the Summary of the Invention on page 3, lines 11-34 with the following amended paragraph:

These and other objects of the invention, which shall become hereafter apparent, are achieved by the present invention, which involves a high speed serial interface that enables communication between the central processing unit (CPU) of a system of playing games of skill or chance or entertainment (a gaming machine) and an input/output control board (IOCB) for controlling peripheral devices associated with the gaming machine. The interface has either an Industry Standard Architecture (ISA) bus, a Universal Serial Bus (USB) or the IEEE 1394 FIREWIRE™ bus. The IOCB facilitates the communications between the game CPU and the peripheral devices. These peripheral devices can be one or more of the following: for example, displays, buttons, coin hoppers, coin mechanisms, bill validators, reel mechanisms, etc., as known to those skilled in the art. Communication with ~~between~~ the game CPU is bi-directional, and can occur simultaneously. Communication uses a framed message transport protocol, which includes a message header, a body containing a virtual device message and a packet validation signature. The message header identifies the intended recipient of the message. The body includes the message for the recipient. The packet validation signature includes a termination code and a means for checking if errors have occurred in the transmission. The game CPU communicates to the gaming peripheral devices by sending the device messages across the ISA bus to the IOCB. The IOCB then routes the device messages to the appropriate device. Use of the IOCB and the high speed

interface enables the game CPU to use more of its available functions for controlling gaming functions rather than the operation of its associated peripheral devices.

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 4, lines 19-12 and page 5, lines 1-14 with the following amended paragraph:

An intelligent input/output control board ("IOCB", "control board") is designed to work in conjunction with gaming machines, such as the video poker machine 10 or slot machine 20 shown in Fig. 1. As will be described below, each of these machines contains a microcomputer board 30 (not shown in Fig. 1) which contains the instructions for operating the games i.e., the game software[[)]]. As shown in Fig. 1, elements common to these machines include a display 11, a coin slot 12, a bill or card (credit card, debit card, other forms of electronic media) acceptor slot 13, a coin hopper/receptacle 14, a plurality of game buttons 15 which may contain lights 16 therein. Each gaming machine offers several ways in which the game player can deposit moneys into the machine, receive change where appropriate[[s]], in order to place bets on the conclusion of the particular game or games. In the case of slot machine 20, a handle 21 is present which can be used to operate the machine. The game buttons, lights and handles offer a means of allowing the player to interact with the gaming device, with the possibility of affecting the game conclusion. Mechanical and electrical components of these machines known to those skilled in the art are not illustrated. Included among the known functions of these gaming machines are the ability of the game to generate a random conclusion, and to offer a variable return play based upon a particular game conclusion and the game conclusions of other gaming devices with which a particular gaming device may be networked. Also, these gaming devices have the ability to vary the

payout, such as paying a progressive jackpot which provides an additional return payout based upon the history of the various game conclusions prior to a particular individual's playing of the game, whether on a specific gaming machine or from one or more gaming machines networked to the specific gaming machine being played. These gaming devices also generate a variety of audio and visual effects, both during game play and between game play. Some other components, known to those skilled in the art and not shown in the drawings, include bells, reel mechanisms, dice mechanisms, wheel mechanisms and feature displays. In addition to their use for playing games of chance, these machines can also be used for playing games of skill, or for entertainment purposes.

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 5, lines 20-30 with the following amended paragraph:

The main game processor 30 system (Fig. 2) described in the present invention is predicated on using an industry standard microcomputer board (MCB) 32 with a standard operating system (OS) 50 combined with a graphical user interface (GUI) 52 (Fig. 2). The MCB 32 has a central processing unit (CPU or microprocessor) 34, (also referred to as the game CPU), memory means 36 including volatile storage means 38 and non-volatile storage means 40, secured memory storage means 42 and nonsecured memory storage means 44. As shown schematically in Fig. 2, operating system 50 and GUI 52 are in communication with appropriate game software 54, with the OS 50, GUI 52 and game software 54 in communication with each other and the game CPU 34. This standardized hardware architecture and OS approach is used for three unique reasons:

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 14, lines 21-23 with the following amended paragraph:

Data transfers between the IOCB and the game ~~COU~~ CPU use the message data port, and a message status port. The message status port has the following construction:

Please delete the paragraph in the Detailed Description of the Preferred Embodiments on page 14, lines 24-26, which begins with "[Assume ...".

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 15, lines 13-20 with the following amended paragraph:

RTT (Ready To Transmit): if the IOCB has data to send, it sets this bit and asserts the interrupt Request to the game CPU. When the interrupt is serviced and the character has been read, the IOCB's hardware is notified via an interrupt, and the IOCB resets this bit if there are no bytes to send from the current message. If there are more bytes to send, the IOCB places the next byte on the message port, without resetting the ready-to-transmit bit and triggers the Interrupt Request to the game CPU.

Please replace the paragraph in the Detailed Description of the Preferred Embodiments from page 16, lines 20-30 to page 17, lines 1-8 with the following amended paragraph:

In the preferred embodiment of the present invention in which the communications link between the game CPU and the IOCB uses either USB or FIREWIRE™, there are no pertinent inter-character time-out. In those embodiments in which the communication link

uses a message port and status flag, message traffic is controlled with time-outs. There is an inter-character time-out within a message that is one or two milliseconds, and there is an inter-message time-out that is three times the inter-character time-out. Because the message port is bi-direction, there is a set of timers for messages going from the IOCB to the game CPU and another set of timers for messages going from the game CPU to the IOCB. Each component, both the IOCB and the game CPU, keeps track of these two timer sets. If the inter-character time-out interval expires, the current message being transferred is in error, and will be aborted (see 458, 462, 464 for the game CPU, in Fig. ~~6a~~ 6b, and 508, 510, 521, for the IOCB in the Fig. 7). If the busy flag 403 is raised while the message is being transferred, the game CPU will give the IOCB an extra five time-out periods before declaring an error and aborting the message transmission (see 403-406[[)]] in Fig. 6a). The inter-character time-out is not cumulative, and is reset after each new character is received (see 418, 424, 465) for the game CPU, in Fig. 6a and ~~416, 428~~ 516, 528, for the IOCB Fig. 7.

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 21, lines 12-14 with the following amended paragraph:

If at 502 the port is being read, and the bit status is not Ready to Transmit(~~RIT~~RTT) at 504, the inter-message timer counter is set at 505 and the IOCB determines if the port is written at 518, as described above.

Please replace the paragraph in the Detailed Description of the Preferred Embodiments on page 21, lines 25-29 with the following amended paragraph:

If at ~~214~~ 514, the number of transmissions is less than the number of transmitted messages, at 516 the IOCB sends a transmit message to the message port, sets the IRQ line to

TRUE, and resets the inter-byte timeout counter. Upon completion of the procedure at reference numeral 516, the IOCB determines if the port is written, at 518, as described above.